亞士晶科技
T-SMARTLINK MICROELECTRONICS

DisplayPort Repeater & HDMI/DVI Level Shifter

Description

TS105 is the high-speed level shift ICs for HDMI and DVI video application. TS105 integrates 1-to-1 DP Repeater & HDMI/DVI Level Shifter to simplify system level design and cost.

TS105 support up to 3.4Gbps bandwidth of pixel data transition, as indicated in HDMI Rev1.4a. This conversion is automatic and transparent to the user. The devices

operate at a single 3.3V supply.

Feature

- DisplayPort Repeating
- HDMI/DVI level shifting operation up to 3.4Gbps per lane
- Support HDMI 2.0 4:2:0 format
- Integrated 50Ω termination resistors for AC-coupled differential inputs.
- DDC/HPD Level Shifting .
- DDC Buffer Support .
- ESD protection up to 6kV.

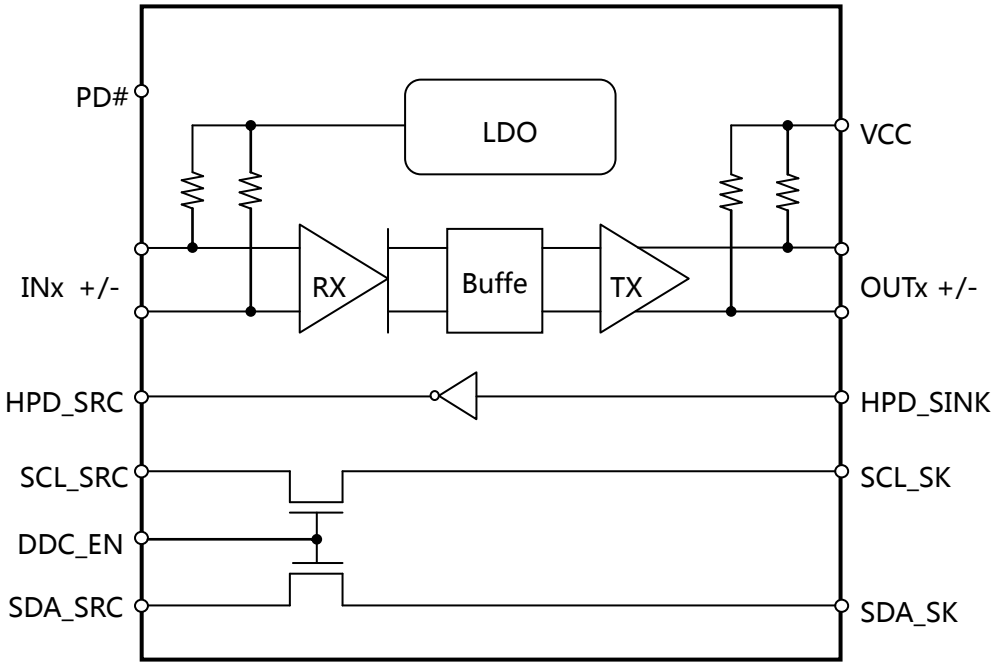
Package

- QFN32 (5*5*0.85)

Power

- Power supply 3.3 V±10 %.
- Power-saving modes by source-side disablement (using output enable) as well as sink-side detection (using Hot Plug Detect).

Function Block



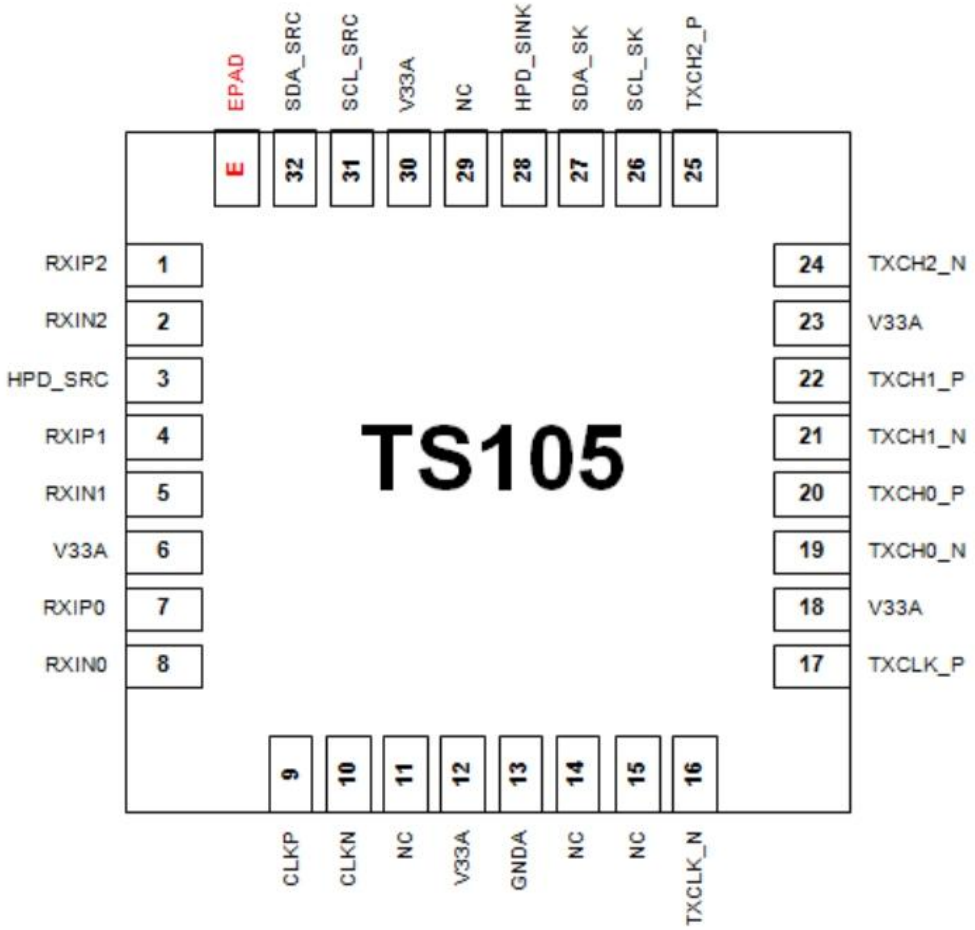
更新纪录

版本	日期	更新信息
Rev 1.0	2021/12	Initial
Rev 1.1	2022/03	Add QFN32 Package
Rev 1.2	2024/05	Remove QFN40 Package

DisplayPort Repeater & HDMI/DVI Level Shifter

Pinout Diagram

QFN32



Pin	Name	Type	Description
1	RXIP2	Input	Positive signal of TMDS differential input from display source.
2	RXIN2	Input	Negative signal of TMDS differential input from display source.
3	HPD_SRC	Output	3.3V HPD detection.
4	RXIP1	Input	Positive signal of TMDS differential input from display source.
5	RXIN1	Input	Negative signal of TMDS differential input from display source.
6	V33A	Power	3.3V± 10% DC Power Supply.
7	RXIP0	Input	Positive signal of TMDS differential input from display source.
8	RXIN0	Input	Negative signal of TMDS differential input from display source.
9	CLKP	Input	Positive signal of TMDS differential input from display source.

10	CLKN	Input	Negative signal of TMDS differential input from display source.
11	NC	-	Reserved.
12	V33A	Power	3.3V± 10% DC Power Supply.

Pin	Name	Type	Description
13	GNDA	GND	Ground.
14	NC	-	Reserved.
15	NC	-	Reserved.
16	TXCLK_N	Output	Negative signal of HDMI compliant TMDS differential output to display sink.
17	TXCLK_P	Output	Positive signal of HDMI compliant TMDS differential output to display sink.
18	V33A	Power	3.3V± 10% DC Power Supply.
19	TXCH0_N	Output	Negative signal of HDMI compliant TMDS differential output to display sink.
20	TXCH0_P	Output	Positive signal of HDMI compliant TMDS differential output to display sink.
21	TXCH1_N	Output	Negative signal of HDMI compliant TMDS differential output to display sink.
22	TXCH1_P	Output	Positive signal of HDMI compliant TMDS differential output to display sink.
23	V33A	Power	3.3V± 10% DC Power Supply.
24	TXCH2_N	Output	Negative signal of HDMI compliant TMDS differential output to display sink.
25	TXCH2_P	Output	Positive signal of HDMI compliant TMDS differential output to display sink.
26	SCL_SK	I/O	5V DDC Clock I/O connecting to sink device.
27	SDA_SK	I/O	5V DDC Data I/O connecting to sink device.
28	HPD_SINK	Input	This signal comes from the HDMI/DVI sink. If HPD_SINK= 1, it indicates“plugged”state; If HPD_SINK= 0, it indicates“unplugged”. HPD_SINK is pulled down by an integrated pull-down resistor.
29	NC	-	Reserved.
30	V33A	Power	3.3V± 10% DC Power Supply.
31	SCL_SRC	I/O	3.3V DDC Clock I/O connecting to sink device.

32	SDA_SRC	I/O	3.3V DDC Data I/O connecting to sink device.
E	EPAD	-	Must connect to ground.

Electrical Characteristics

Parameter	Symbols	Min.	Nom.	Max.	UNIT
Recommended Operating Conditions					
3.3V Power Supply	VDD	3.0	3.3	3.6	V
3.3V Supply Current	IDD	-	-	100	mA
Operating temperature range	T	-	-	85	°C
IDD @ Operating (165MHz)	IOP	-	-	100	mA
Electrical Characteristics for IN[4:1]+/-					
Unit Interval	T_{BIT}	360	-	-	ps
Differential Input Peak to Peak Voltage	$V_{RX-Diffp-p}$	-	-	1.2	V
Minimum Eye Width at INx input pair	T_{RX-EYE}	0.8	-	-	Tbit
AC Peak Common-Mode Input Voltage	$V_{CM-AC-pp}$	-	-	100	mV
DC Input Impedance	Z_{RX-DC}	40	50	60	Ω
Rx Input Termination Voltage	$V_{RX-Bias}$	0	-	2	V
Single-end input resistance for INx when inputs are in high-Z state	$Z_{RX-HIGH-Z}$	100	-	-	kΩ
Electrical Characteristics for OUT[4:1]+/-					
Single-ended high-level output voltage	V_H	AVCC - 10mV	AVCC	AVCC + 10mV	V
Single-ended low-level output voltage	V_L	AVCC - 600mV	AVCC - 500mV	AVCC - 400mV	V
Single-ended output swing voltage	V_{SWING}	400	500	600	mV
Single-ended current in high-Z state	I_{OFF}	-	-	10	uA
Rise Time	T_R	125	-	$0.4T_{BIT}$	ps
Fall Time	T_F	125	-	$0.4T_{BIT}$	ps
Intra-pair differential skew	T_{SKEW_INTRA}	-	-	10	ps
Inter-pair lane-to-lane output skew	T_{SKEW_INTER}	-	-	250	ps
Jitter added to TMDS signals	T_{JIT}	-	-	25	ps

Parameter	Symbols	Min.	Nom.	Max.	UNIT
Electrical Characteristics for PD# and DDC_EN					
Input High Level	V_{IH}	2	-	VDD	V
Input Low Level	V_{IL}	0	-	0.8	V
Input Leakage Current	I_{IN}	-	-	10	uA
Electrical Characteristics for HPD_SINK and HPD_SRC					
HPD_SINK Input High Level	$V_{IH\_HPD\_SINK}$	2	5	5.5	V
HPD_SINK Input Low Level	$V_{IL\_HPD\_SINK}$	0	-	0.8	V
HPD_SINK Input Leakage Current	$I_{IN\_HPD\_SINK}$	-	-	50	uA
HPD_SRC Output High-Level	$V_{OH\_HPD\_SRC}$	3	-	3.6	V
HPD_SRC Output Low-Level	$V_{OL\_HPD\_SRC}$	0	-	0.2	V
HPD_SINK to HPD_SRC propagation delay	T_{HPD}	-	-	200	ps
HPD_SRC rise/fall time	T_{RF-HPD_SRC}	1	-	20	ns
HPD_SINK Input Pull-down Resistor	R_{HPD}	100	200	300	kΩ
Electrical Characteristics for SDA, SCL, SDA_SINK and SCL_SINK					
Input Voltage	V_{I-DDC}	0	-	5.5	V
Input Leakage	I_{LK-DDC}	-	-	10	uA
Input / output capacitance	C_I	-	-	10	pF
Switch resistance	R_{ON}	-	-	50	Ω

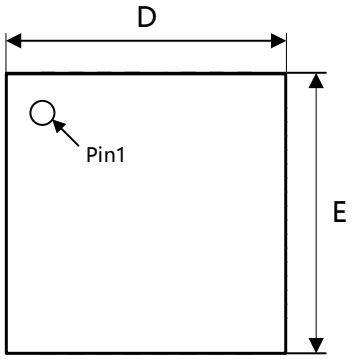
Absolute Maximum Ratings

Parameter	Range
Power Supply	-0.5V to 3.6V
DC Input Voltage	-0.5V to 3.6V
Output Voltage	-0.5V to 3.6V
Storage Temperature	-55℃ to 150℃
Operation Temperature	0℃ to 85℃
ESD HBM	± 6KV

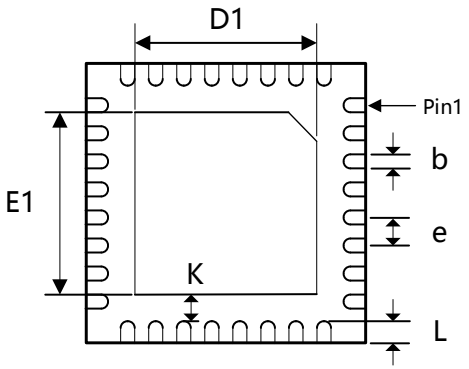
Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Package

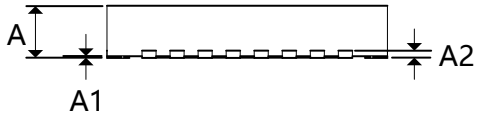
QFN32



TOP-VIEW



BOTTOM-VIEW



SIDE-VIEW

Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.83	0.85	0.88
A1	0.00	-	0.05
A2	0.203REF		
b	0.23	0.25	0.27
D	4.95	5.00	5.05
D1	3.60	3.65	3.70
E	4.95	5.00	5.05
E1	3.60	3.65	3.70
e	0.48	0.50	0.52
K	0.33REF		
L	0.30	0.35	0.40

PCB Layout Guideline

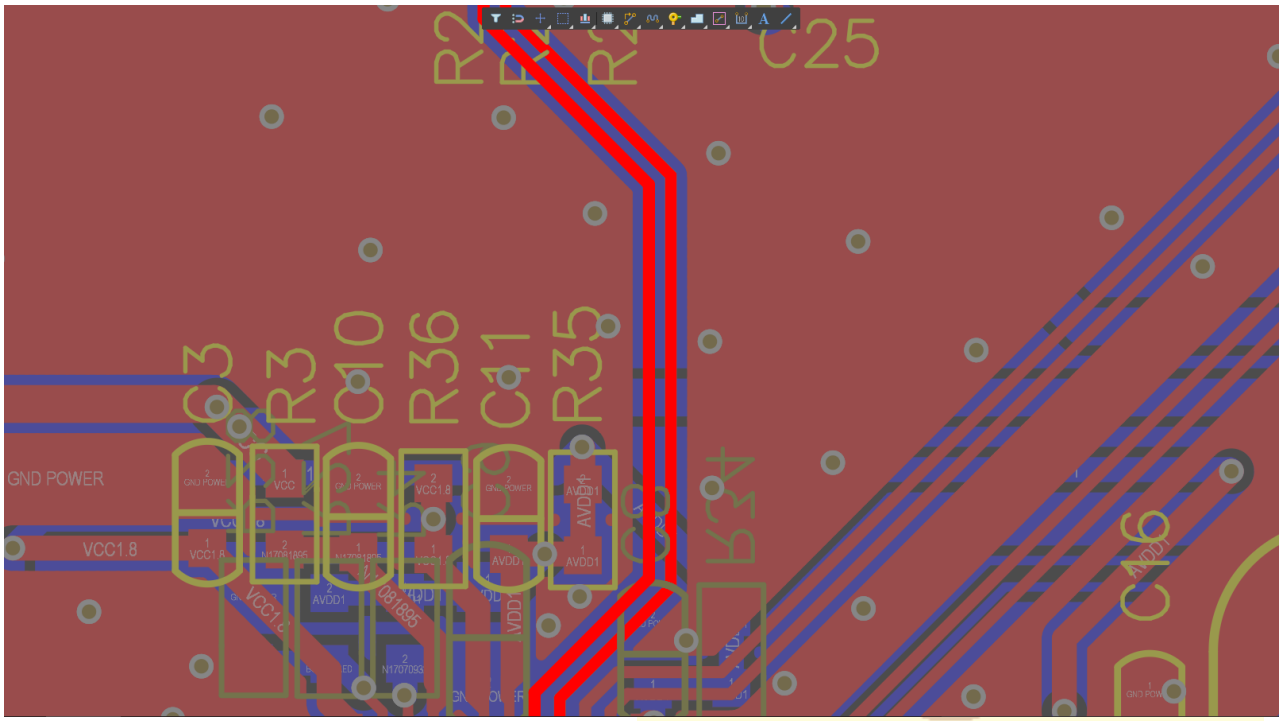
A. Principle of Impedance control

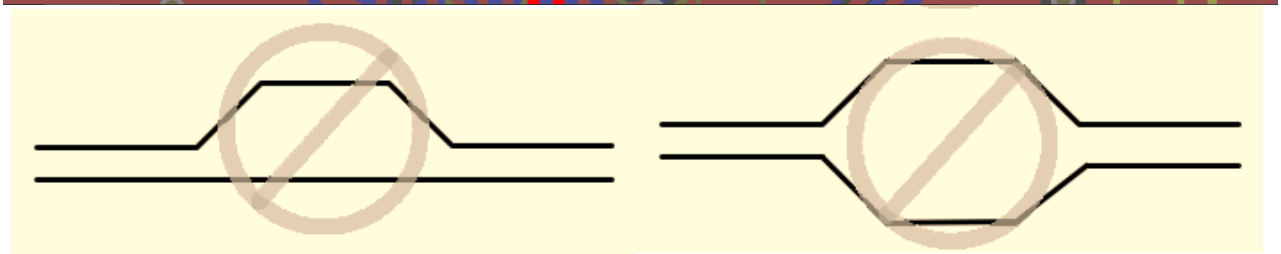
The length of intra-pair should be equal and the pair of trace should be routed closely. Components or Via on differential channel must be placed symmetrically. The distance between two traces of the differential pair must remain constant from beginning to the end. Calculations of differential impedance are necessary for differential signals and traces.

- HDMI the differential trace impedance: 100 ohm +/- 15%
- Display Port the differential trace impedance: 100 ohm +/- 15%
- USB 2.0 the differential trace impedance: 90 ohm +/- 15%
- USB Type-C the differential trace impedance: 90 ohm +/- 15%

B. Symmetry in the Differential Pairs

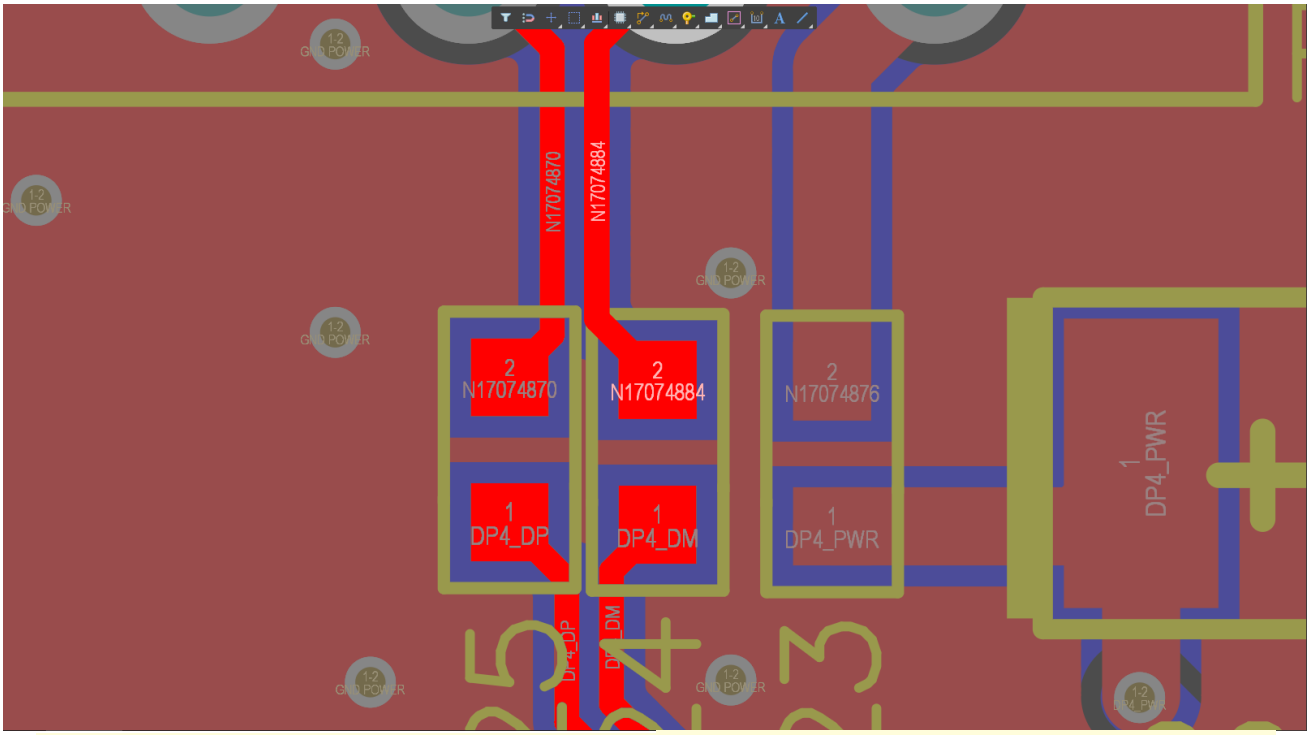
Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short.

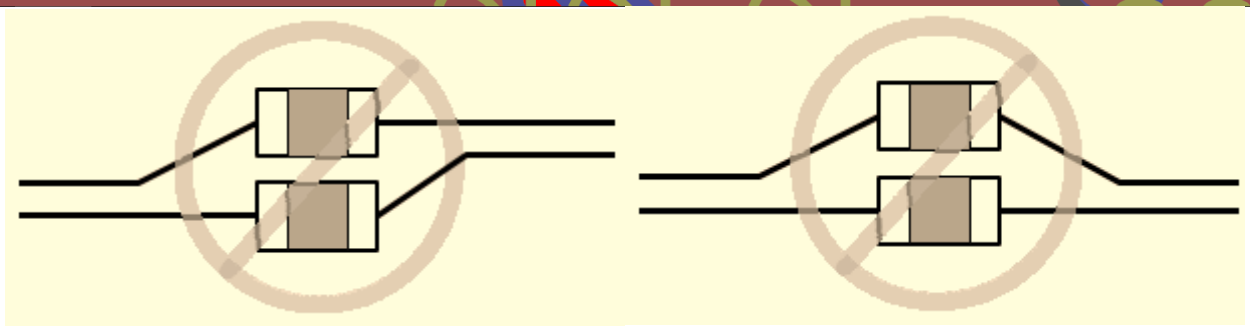




C. Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. It is strongly recommended use 0402 or smaller size. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement.





D. Exposed Pad (ePad)

ExposedPad (ePad) is used as electrical ground of the package for applications requiring optimum thermal performance. Soldering the ePad on to the ground plane of PCB is required to

fulfill package power dissipation requirement. A clearance on the PCB between the edge of ePad and the inner edges of lead Pads should be designed at least 0.25 mm to avoid electrical short.