亞士晶科技
T-SMARTLINK MICROELECTRONICS

HDMI/DVI Switch (3:1)

Description

The TS106 is 3-Port HDMI/DVI switch that is targeted for high-resolution video networks that are based on HDMI 1.4 and DVI 1.0 specifications. Multiple HDMI/DVI ports allow consumers to connect variety HDMI/DVI sources to their HDTV.

The TS106 switch selects a single HDMI/DVI signal from the three receiver ports and generates fully compliant HDMI/DVI audio/video output, as well as DDC and HPD switching in full compliance with the HDMI/DVI specifications.

The TS106 integrate DDC switch, HPD switch and RX-side ODTs to enhanced performance, reduce the cost of manufacture and simplify the routing on the system board.

Feature

- HDMI 1.4/DVI 1.0 compliant.
- Supports data rates up to 3.4Gbps.
- Supports deep color.
- RX side ODTs and management circuitry
- Integrated HPD switch, DDC switch, and +5V Power indicator switch, greatly lowering the cost and simplifying the manufacturing process.
- Source/Sink connection detection for flexible system management.
- I2C control supported.
- Low added jitter.

Package

- QFN64 (7.5×7.5×0.85).

Power

- Power supply 3.3 V±10 %.
- 5V-tolerant DDC interfaces.

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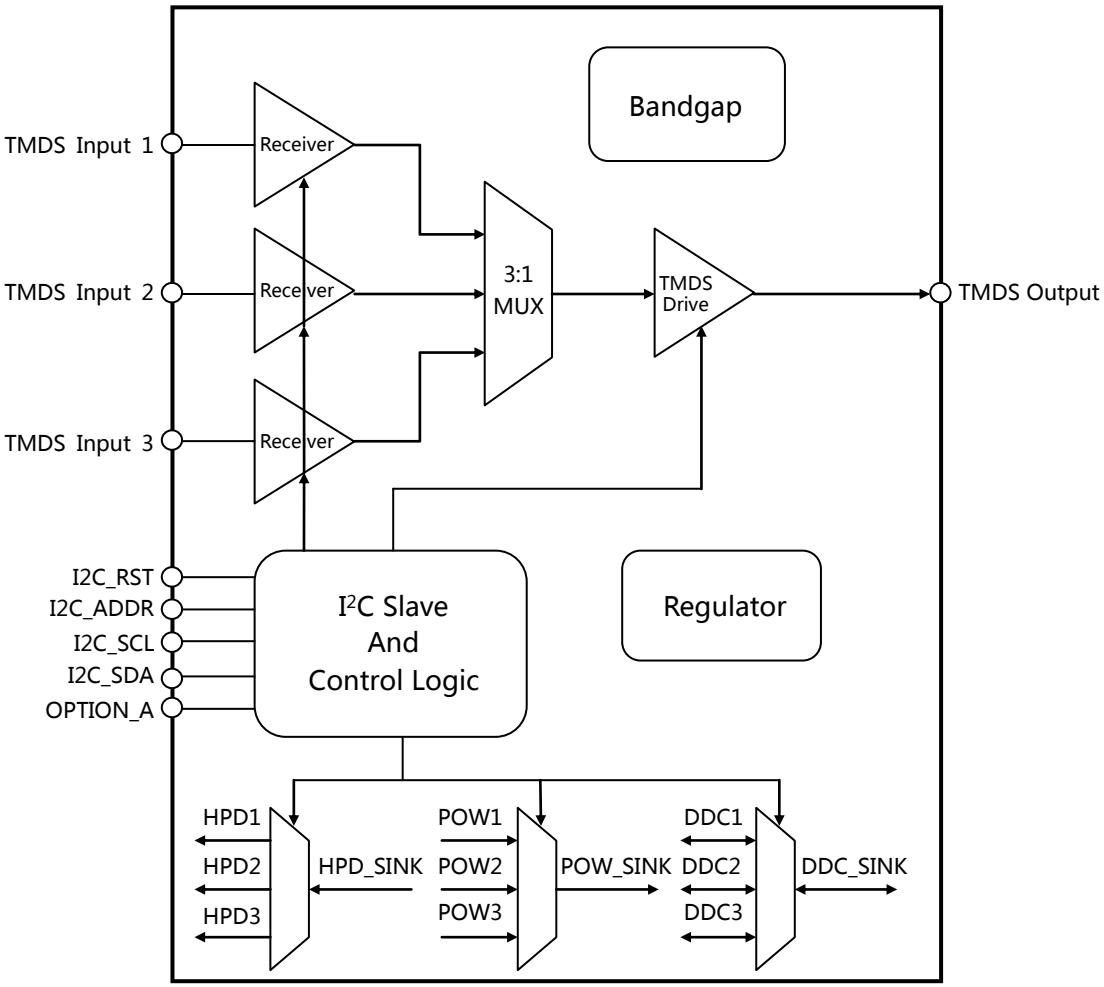
更新纪录

版本	日期	更新信息
Rev 1.0	2021/12	初版
Rev 1.1	2022/03	Correct operation temperature
Rev 1.2	2022/03	Correct parameter
Rev 1.3	2022/09	Add I2C Register

HDMI/DVI Switch (3:1)

Function Block



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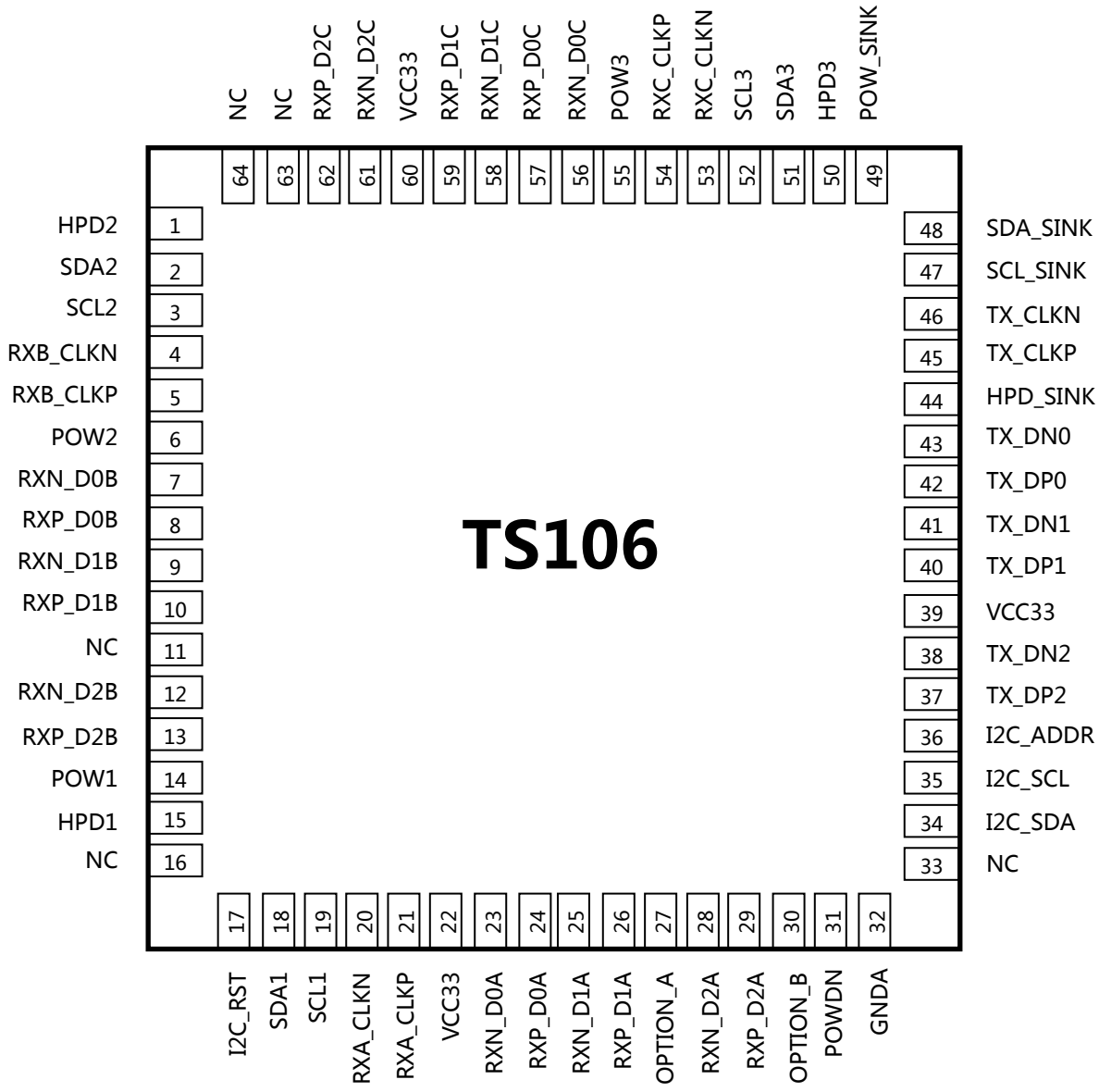
Pinout Diagram



Pin	Name	Type	Description
1	HPD2	I/O	A high value indicates that the sink is connected.
2	SDA2	I/O	Port2 DDC data.
3	SCL2	I/O	Port2 DDC clock.

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4	RXB_CLKN	Input	Port2 TMDS negative inputs.
5	RXB_CLKP	Input	Port2 TMDS positive inputs.

Pin	Name	Type	Description
6	POW2	Input	Port2 5V Power Input.
7	RXN_D0B	Input	Port2 TMDS negative inputs.
8	RXP_D0B	Input	Port2 TMDS positive inputs.
9	RXN_D1B	Input	Port2 TMDS negative inputs.
10	RXP_D1B	Input	Port2 TMDS positive inputs.
11	NC	Output	Function test pin, please keep floating
12	RXN_D2B	Input	Port2 TMDS negative inputs.
13	RXP_D2B	Input	Port2 TMDS positive inputs.
14	POW1	Input	Port1 5V Power Input.
15	HPD1	I/O	A high value indicates that the sink is connected.
16	NC	Output	Function test pin, please keep floating
17	I2C_RST	I/O	Chip reset pin, high active, internal pull low.
18	SDA1	I/O	Port1 DDC data.
19	SCL1	I/O	Port1 DDC data.
20	RXA_CLKN	Input	Port1 TMDS negative inputs.
21	RXA_CLKP	Input	Port1 TMDS positive inputs.
22	VCC33	Power	3.3V Power Supply.
23	RXN_D0A	Input	Port1 TMDS negative inputs.
24	RXP_D0A	Input	Port1 TMDS positive inputs.
25	RXN_D1A	Input	Port1 TMDS negative inputs.
26	RXP_D1A	Input	Port1 TMDS positive inputs.
27	OPTION_A	Input	Channel switch button input, low active, internal pull high.
28	RXN_D2A	Input	Port1 TMDS negative inputs.
29	RXP_D2A	Input	Port1 TMDS positive inputs.
30	OPTION_B	Input	Test pin.
31	POWDN	Input	Chip power down control pin, high active.
32	GNDA	GND	Ground.
33	NC	-	

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34	I2C_SDA	I/O	Configuration I2C SDA line.
35	I2C_SCL	I/O	Configuration I2C SCL line.
36	I2C_ADDR	I/O	Configuration I2C device address selection pin.

Pin	Name	Type	Description
37	TX_DP2	Output	TMDS positive output.
38	TX_DN2	Output	TMDS negative output.
39	VCC33	Power	3.3V Power Supply.
40	TX_DP1	Output	TMDS positive output.
41	TX_DN1	Output	TMDS negative output.
42	TX_DP0	Output	TMDS positive output.
43	TX_DN0	Output	TMDS negative output.
44	HPD_SINK	Input	Sink side hot plug detector input.
45	TX_CLKP	Output	TMDS positive output.
46	TX_CLKN	Output	TMDS negative output.
47	SCL_SINK	I/O	Sink side DDC clock.
48	SDA_SINK	I/O	Sink side DDC data.
49	POW_SINK	Output	Sink side POW.
50	HPD3	I/O	A high value indicates that the sink is connected.
51	SDA3	I/O	Port3 DDC data.
52	SCL3	I/O	Port3 DDC clock.
53	RXC_CLKN	Input	Port3 TMDS negative inputs.
54	RXC_CLKP	Input	Port3 TMDS positive inputs.
55	POW3	Input	Port3 5V Power Input.
56	RXN_D0C	Input	Port3 TMDS negative inputs.
57	RXP_D0C	Input	Port3 TMDS positive inputs.
58	RXN_D1C	Input	Port3 TMDS negative inputs.
59	RXP_D1C	Input	Port3 TMDS positive inputs.
60	VCC33	Power	3.3V Power Supply.
61	RXN_D2C	Input	Port3 TMDS negative inputs.
62	RXP_D2C	Input	Port3 TMDS positive inputs.

63	NC	Output	Function test pin, please keep floating
64	NC	-	

Electrical Characteristics

Parameter	Symbols	Min.	Nom.	Max.	UNIT
Normal Operating Conditions					
3.3V Power Supply	VCC33	3.0	3.3	3.6	V
Operating temperature range	T_{OP}			70	℃
IDD @ Operating (165MHz)	IOP		200		mA
IDD @ Power Down	IPD		3		mA
CML Inputs					
Differential Input Voltage Swing	V_{IN_DIFF}	150	1000	1200	mVp-p
Common-Mode Input Voltage	V_{IN_COM}	VCC33 -0.5		VCC33 +0.1	V
Input Resistance (Single-end)	R_{IN_SE}	45	50	55	Ω
CML Output					
Differential Output Voltage Swing (50Ω load)	V_{OUT_50ohm}	800	1000	1400	mVp-p
Output Voltage High (Single-end)	$V_{OUT\_High\_SE}$		VCC33		mV
Output Voltage Low (Single-end)	$V_{OUT\_Lpw\_SE}$	VCC33 -600		VCC33 -400	mV
Output Voltage (Power Down, Single end)	$V_{OUT\_PD\_SE}$	VCC33 -10		VCC33 +10	mV
Common-Mode Output Voltage (50Ω load)	V_{OUT_COM}		VCC33-0.25		V
Rise/Fall Time (20% to 80%)	T_{RISE}/T_{FALL}	80	130	200	ps
TTL Control and Status Interface					
TTL Input High Voltage	V_{TTL_IH}	2			V
TTL Input Low Voltage	V_{TTL_IL}			0.8	V
DDC Output High Voltage	V_{DDC_OH}	2.4			V
DDC Output Low Voltage	V_{DDC_OL}			0.4	V

Absolute Maximum Ratings

Parameter	Range
Power Supply	-0.3V to 3.6V
DC Input Voltage	-0.3V to 3.6V
Output Voltage	-0.3V to 3.6V
Storage Temperature	-40℃ to 125℃
Operation Temperature	0℃ to 70℃
ESD HBM	± 4.5KV

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

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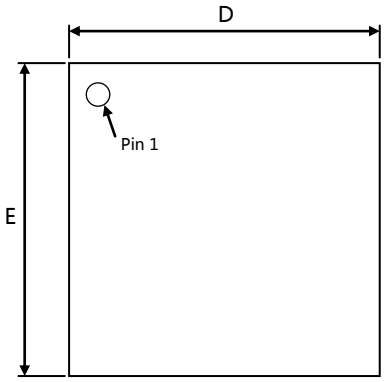
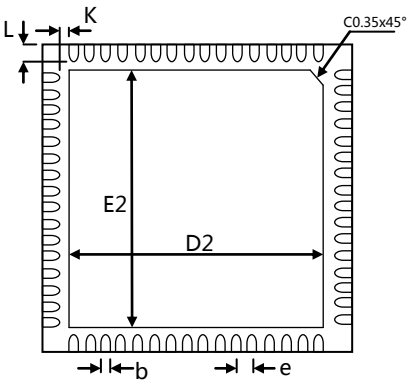
Package

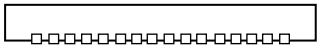
QFN64(7.5*7.5)



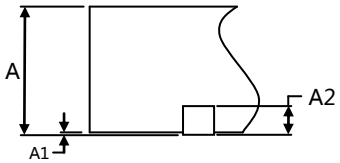
TOP-VIEW



BOTTOM-VIEW



FRONT-VIEW



DETAIL-VIEW

Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.83	0.85	0.88
A1	0.00	0.02	0.05
A2		0.203Ref	
b	0.20	0.20	0.25
D	7.45	7.50	7.55
D2	6.15	6.20	6.25
E	7.45	7.50	7.55
E2	6.15	6.20	6.25
e	0.35	0.40	0.45
K		0.25Ref	
L	0.35	0.40	0.55

PCB Layout Guideline

A. Principle of Impedance control

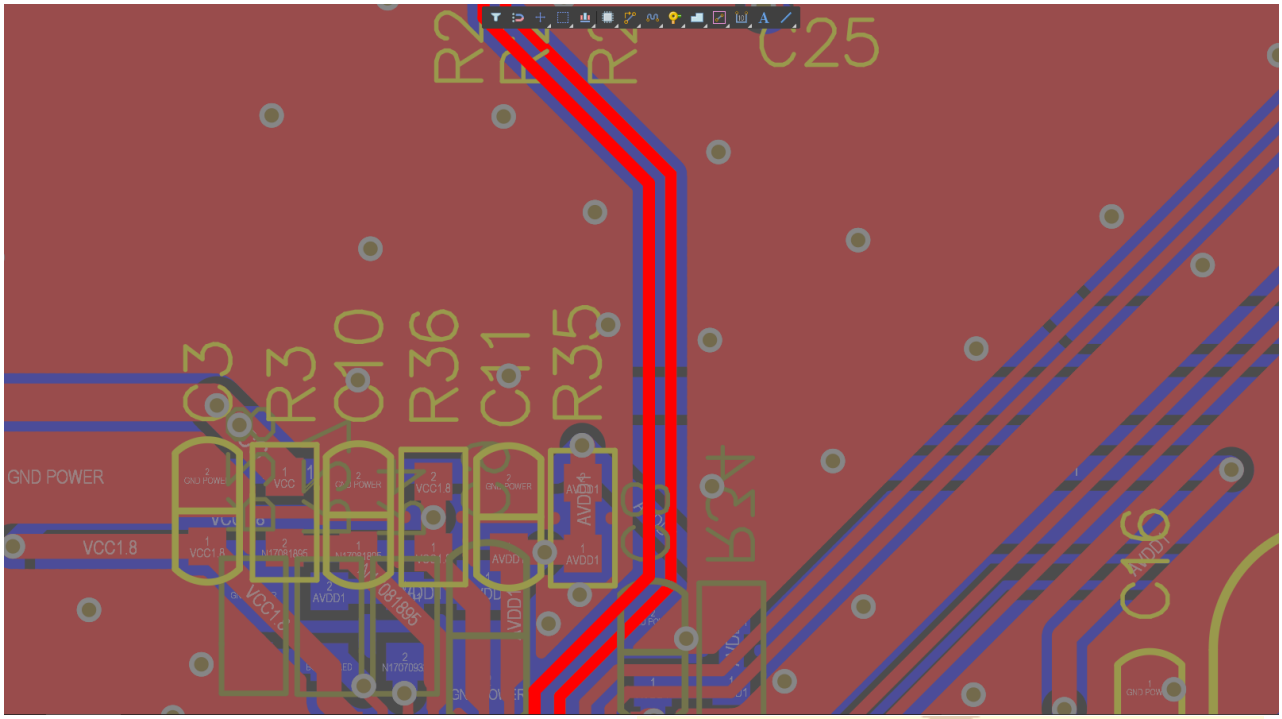
The length of intra-pair should be equal and the pair of trace should be routed closely. Components or Via on differential channel must be placed symmetrically. The distance between two traces of the differential pair must remain constant from beginning to the end. Calculations of differential impedance are necessary for differential signals and traces.

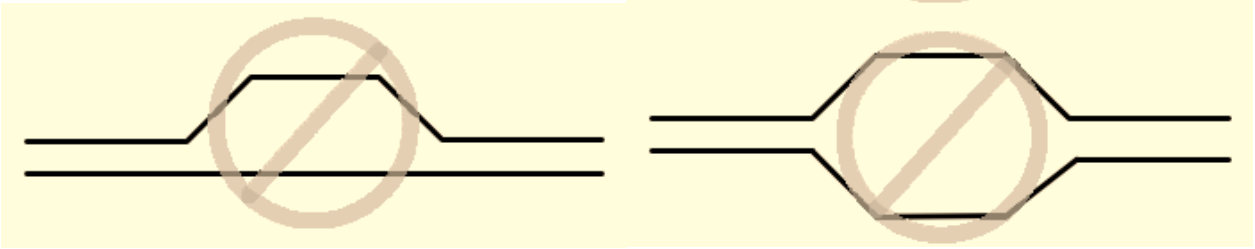
- HDMI the differential trace impedance: 100 ohm +/- 15%
- Display Port the differential trace impedance: 100 ohm +/- 15%

- USB 2.0 the differential trace impedance: 90 ohm +/- 15%
- USB Type-C the differential trace impedance: 90 ohm +/- 15%

B. Symmetry in the Differential Pairs

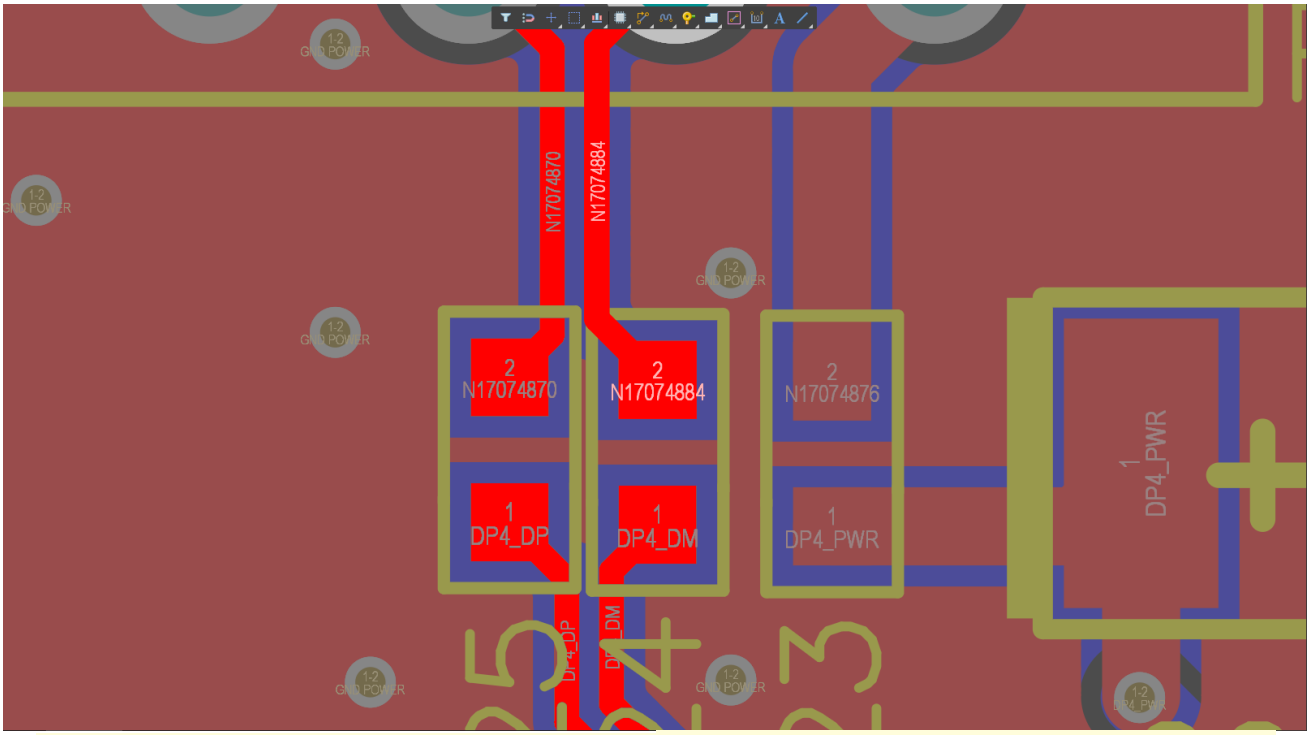
Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short.

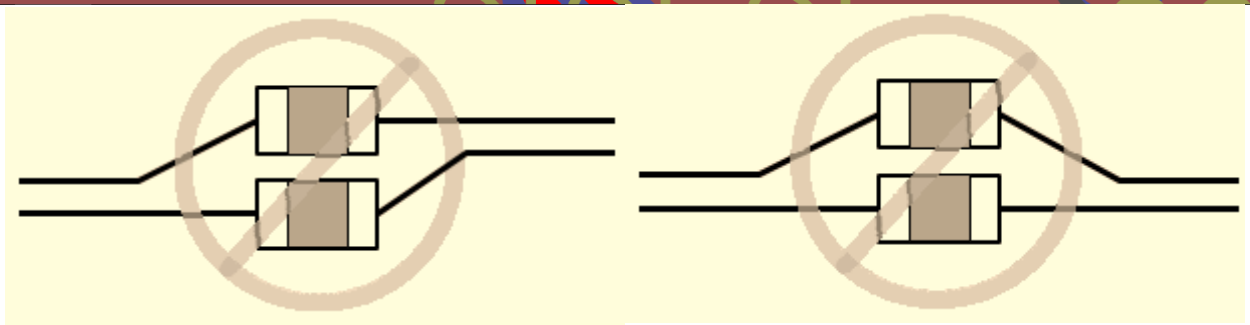




C. Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. It is strongly recommended use 0402 or smaller size. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement.





D. Exposed Pad (ePad)

ExposedPad (ePad) is used as electrical ground of the package for applications requiring optimum thermal performance. Soldering the ePad on to the ground plane of PCB is required to

fulfill package power dissipation requirement. A clearance on the PCB between the edge of ePad and the inner edges of lead Pads should be designed at least 0.25 mm to avoid electrical short.

I2C Register

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0x19	8'h04	2:0	MUXV[2:0]	R/W	3X1 MUX gate voltage setting, default=[100]
		3	TXODT_OFF	R/W	TX termination off when "1" (default "0")
		4	CHSA	R/W	Channel selection
		5	CHSB	R/W	Channel selection
		6	CHSC	R/W	Channel selection
		7	CHANNEL_SEL_ OPTION	R/W	Channel select option (default"0") 0: hardware auto select 1: use register setting value

